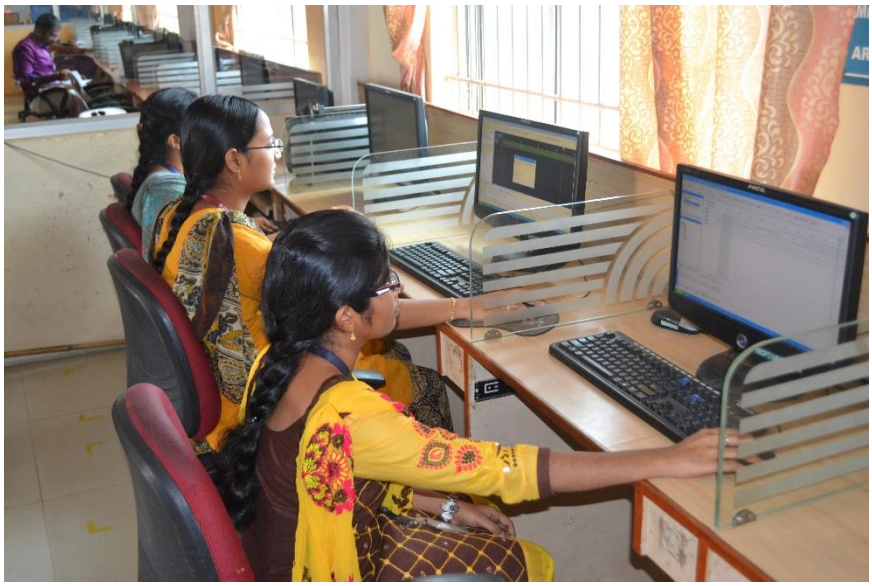
VLSI DESIGN LABORATORY

Laboratory In- charge: Mrs.D.Dharini AP/ECE

Technical supporting staff: Mr. M. Hariharan



Snapshot of VLSI Design Laboratory

Area of the laboratory: 104.96 Sq.m

Major Equipment:

- Personal Computer - INTEL PENTIUM DUAL CORE
- SPARTAN 3 Universal Multivendor Kit
- Interfacing Card-1 Traffic Controller Card
- Interfacing Card-2
- 7-Segment Display Interface Card
- CADENCE UNIVERSITY BUNDLE
- SPARTAN 6 Trainer kit
- CYCLONE IV Trainer Kit

List of Experiments:

- HDL based design entry and simulation of simple counters, state machines, adders (min 8 bit) and multipliers
- Synthesis, P&R and post P&R simulation of the components
- Hardware fusing and testing of each of the blocks using either chipscope feature (Xilinx) or the signal tap feature (Altera)
- Invoke the PLL and demonstrate the use of the PLL module for clock generation in FPGAs
- Design and simulation of a simple 5 transistor differential amplifier. Measure gain, ICMR, and CMRR
- Layout generation, parasitic extraction and resimulation of the circuit
- Synthesis and Standard cell based design of an circuits
- Identification of critical paths, power consumption
- P&R, power and clock routing, and post P&R simulation
- Analysis of results of static timing analysis

Beyond the syllabus experiments:

- Basic Gates Implementation using GDI (Cadence)

Utilization of the laboratory:

- VLSI Design Laboratory for III year ECE/VI sem